Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-42 (Canceled)

Claim 43 (Currently amended): A tested semiconductor device produced by a process comprising ~~the steps of~~:

providing a wafer having a plurality of semiconductor devices thereon, each of said semiconductor devices including a plurality of electrical contact terminals;

~~providing a probe card assembly,~~ adjusting a planar orientation of probe elements of a probe card assembly to correspond to a planar orientation of said electrical contact terminals, said probe card assembly comprising:

a probe card having a plurality of electrical contacts,

a probe substrate having ~~a plurality of~~ said probe elements,

a compliant electrical connection electrically connecting said probe card with said probe substrate, said compliant electrical connection allowing relative movement between said probe card and said probe substrate while maintaining electrical connections between said probe card and said probe substrate, and

a moveable element disposed to alter an orientation of said probe substrate with respect to said probe card;

~~contacting said wafer and said probe card assembly such that~~ effecting contact between ones of said electrical contact terminals of said semiconductor devices ~~are in electrical contact with~~ and ones of said probe elements; and

testing said semiconductor devices.

Claims 44-47 (Canceled)

Claim 48 (Previously presented): The tested semiconductor device of claim 43, wherein the process further comprises dicing said wafer to singulate said semiconductor devices.

Claim 49 (Previously presented): The tested semiconductor device of claim 43, wherein said probe substrate comprises a space transformer.

Claim 50 (Canceled)

Claim 51 (Previously presented): The tested semiconductor device of claim 43, wherein said moveable element comprises a threaded element.

Claim 52 (Previously presented): The tested semiconductor device of claim 43, wherein said moveable element comprises a screw.

Claim 53 (Previously presented): The tested semiconductor device of claim 52, wherein said screw comprises a differential screw.

Claim 54 (Previously presented): The tested semiconductor device of claim 43, wherein moving said moveable element in a first direction causes at least a portion of said probe substrate to move toward said probe card.

Claim 55 (Previously presented): The tested semiconductor device of claim 54, wherein moving said moveable element in a second direction allows at least a portion of said probe substrate to move away from said probe card.

Claim 56 (Previously presented): The tested semiconductor device of claim 43, wherein said moveable element comprises a servo mechanism disposed to alter a position of said probe substrate with respect to said probe card.

Claim 57 (Previously presented): The tested semiconductor device of claim 43, wherein said moveable element comprises a piezoelectric actuator disposed to alter a position of said probe substrate with respect to said probe card.

Claim 58 (Canceled)

Claim 59 (Previously presented): The tested semiconductor device of claim 43, wherein said probe elements are elongate and resilient.

Claim 60 (Previously presented): The tested semiconductor device of claim 43, wherein said moveable element is capable of planarizing tips of said probe elements with respect to said electrical contact terminals of said semiconductor device.

Claim 61 (Previously presented): The tested semiconductor device of claim 43, wherein said moveable element comprises a pivot structure.

Claim 62 (Previously presented): The tested semiconductor device of claim 61, wherein said pivot structure is disposed against said probe substrate.

Claim 63 (Previously presented): The tested semiconductor claim 43, wherein said moveable element comprises a sphere.

Claim 64 (Previously presented): The tested semiconductor device of claim 43, wherein said moveable element comprises a differential screw that comprises an outer threaded portion and an inner threaded portion.

Claim 65 (Previously presented): The tested semiconductor device of claim 43, wherein said probe substrate is mounted to said probe card by a means that is different than said moveable element.

Claims 66-73 (Canceled)

Claim 74 (Previously presented): The tested semiconductor device of claim 43 wherein:
said probe substrate is mounted to said probe card with a biasing force, and
said moveable element is configured to apply a force in opposition to said biasing force.

Claim 75 (Previously presented): The tested semiconductor device of claim 99, wherein:

said interposer comprises a substrate and a plurality of conductive vias passing through said substrate, and

one elongate interconnection element in each of said pairs of elongate interconnection elements is electrically connected to one end of one of said vias and said other elongate interconnection element in each of said pairs of elongate interconnection elements is electrically connected to an opposite end of said one of said vias.

Claim 76 (Previously presented): The tested semiconductor device of claim 75, wherein:

said interposer further comprises a plurality of first terminals disposed on a first side of said interposer and a plurality of second terminals disposed on a second side of said interposer,

ones of said vias electrically connect ones of said first terminals with ones of said second terminals, and

said one elongate interconnection element in each of said pairs of elongate interconnection elements is attached to one of said first terminals and said other elongate interconnection element in each of said pairs of elongate interconnection elements is attached to one of said second terminals.

Claim 77 (Previously presented): The tested semiconductor device of claim 43, further comprising a plurality of conductive passages through said probe substrate, and wherein:

ones of said probe elements are electrically connected to one end of ones of said conductive passages,

one elongate interconnection element in each of said pairs of elongate interconnection elements is in electrical contact with an opposite end of said ones of said conductive passages, and

said other elongate interconnection element in each of said pairs of elongate interconnection elements is in electrical contact with one of said electrical contacts of said probe card.

Claim 78 (Previously presented): The tested semiconductor device of claim 97 further comprising fastening means for moveably fastening said probe substrate to said probe card, wherein said interposer floatingly engages said probe card and said probe substrate without being fastened to said probe substrate or said probe card.

Claim 79 (Previously presented): The tested semiconductor device of claim 99, wherein only tips of said elongate interconnection elements of said interposer touch said probe card or said probe substrate.

Claim 80 (Currently amended): The tested semiconductor device of claim 43, wherein said ~~step of contacting said wafer~~ effecting contact comprises bringing said ones of said probe elements into contact with said ones of said electrical contact terminals of said semiconductor devices.

Claim 81 (Previously presented): The tested semiconductor device of claim 43, wherein said moveable element is capable of altering a planar orientation of said probe substrate with respect to a planar orientation of said probe card.

Claim 82 (Currently amended): A tested semiconductor device produced by a process comprising ~~the steps of~~:

providing a wafer having a plurality of semiconductor devices thereon, each of said semiconductor devices including a plurality of electrical contact terminals;

~~providing a probe card assembly,~~ adjusting a planar orientation of probe elements of a probe card assembly to correspond to a planar orientation of said electrical contact elements, said probe card assembly comprising:

a probe card having a plurality of electrical contacts,

a probe substrate having a plurality of probe elements,

a compliant electrical connection electrically connecting said probe card with said probe substrate, said compliant electrical connection allowing relative movement between said probe card and said probe substrate while maintaining electrical connections between said probe card and said probe substrate, and

means for altering an orientation of said probe substrate with respect to said probe card;

~~contacting said wafer and said probe card assembly such that~~ effecting contact between ones of said electrical contact terminals of said semiconductor devices ~~are in electrical contact with~~ and ones of said probe elements; and

testing said semiconductor devices.

Claim 83 (Previously presented): The tested semiconductor device of claim 82, wherein said means for altering alters a planar orientation of said probe substrate with respect to a planar orientation of said probe card.

Claim 84 (Currently amended): The tested semiconductor device of claim 82, wherein said ~~method further~~ adjusting comprises adjusting a planarity of said probe elements of said probe substrate using said means for altering.

Claim 85 (Currently amended): The tested semiconductor device of claim 84, wherein said adjusting [[step]] further comprises adjusting said planarity of said probe elements of said probe substrate with respect to an expected planarity of said electrical contact terminals of said semiconductor devices.

Claim 86 (Currently amended): The tested semiconductor device of claim 84, wherein said adjusting [[step]] further comprises leveling said probe elements of said probe substrate with respect to an expected planarity of said electrical contact terminals of said semiconductor devices.

Claim 87 (Previously presented): The tested semiconductor device of claim 82, wherein said compliant electrical connection comprises an interposer disposed between said probe card and said probe substrate.

Claim 88 (Previously presented): The tested semiconductor device of claim 87, wherein said electrical connections between said probe card and said probe substrate pass through said interposer.

Claim 89 (Previously presented): The tested semiconductor device of claim 87, wherein said interposer comprises a plurality of paired elongate interconnection elements extending from opposite sides of said interposer, said paired interconnection elements providing said electrical connections between said probe card and said probe substrate.

Claim 90 (Previously presented): The tested semiconductor device of claim 82, wherein each said probe element comprises a spring, whereby said probe elements provide individual compliance with respect to said contact terminals of said semiconductor devices and said means for altering provides global planarization of said probe elements with respect to said contact terminals.

Claim 91 (Previously presented): The tested semiconductor device of claim 82, wherein said compliant electrical connection comprises springs configured to exert a first force against said probe card and a second force against said probe substrate.

Claim 92 (Previously presented): The tested semiconductor device of claim 91, wherein said springs of said compliant electrical connection are electrically conductive and provide said electrical connections between said probe card and said probe substrate.

Claim 93 (Currently amended): The tested semiconductor device of claim 43, wherein said ~~method~~ adjusting further comprises adjusting a planarity of said probe elements of said probe substrate by moving said moveable element.

Claim 94 (Currently amended): The tested semiconductor device of claim 93, wherein said adjusting [[step]] further comprises adjusting said planarity of said probe elements of said probe substrate with respect to an expected planarity of said electrical contact terminals of said semiconductor devices.

Claim 95 (Currently amended): The tested semiconductor device of claim 93, wherein said adjusting [[step]] further comprises leveling said probe elements ~~of said probe substrate~~ with respect to an expected planarity of said electrical contact terminals of said semiconductor devices.

Claim 96 (Previously presented): The tested semiconductor device of claim 43, wherein each said probe element comprises a spring, whereby said probe elements provide individual compliance with respect to said contact terminals of said semiconductor devices and said moveable element provides global planarization of said probe elements with respect to said contact terminals.

Claim 97 (Previously presented): The tested semiconductor device of claim 43, wherein said compliant electrical connection comprises an interposer disposed between said probe card and said probe substrate.

Claim 98 (Previously presented): The tested semiconductor device of claim 97, wherein said electrical connections between said probe card and said probe substrate pass through said interposer.

Claim 99 (Previously presented): The tested semiconductor device of claim 97, wherein said interposer comprises a plurality of paired elongate interconnection elements extending from opposite sides of said interposer, said paired interconnection elements providing said electrical connections between said probe card and said probe substrate.

Claim 100 (Previously presented): The tested semiconductor device of claim 43, wherein said compliant electrical connection comprises springs configured to exert a first force against said probe card and a second force against said probe substrate.

Claim 101 (Previously presented): The tested semiconductor device of claim 100, wherein said springs of said compliant electrical connection are electrically conductive and provide said electrical connections between said probe card and said probe substrate.